JB/Reply Brief
5/21/04

Docket No. AT9-99-287 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Cohen et al.** §
§
Serial No.: **09/377,642** §
§
Filed: **August 19, 1999** §
§
For: **Method and Apparatus for Performing Raster Operations in a Data Processing System** §

Group Art Unit: **2676**

Examiner: **Tung, Kee M.**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

Certificate of Mailing Under 37 C.F.R. § 1.8(a)
I hereby certify this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 11, 2004.

By: Amelia Turner
Amelia C. Turner

APPELLANT'S REPLY BRIEF (37 C.F.R. 1.192)

This brief is in furtherance of the Appeal Brief filed in this case on January 15, 2004.

The fees required under § 1.17(c), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

RELATED APPEALS AND INTERFERENCES

The Examiner's Answer states:

> The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interfaces.

Examiner's Answer, dated March 8, 2004. It is unclear whether the Examiner's Answer is stating that the brief does **not** contain a statement or that a statement **is contained**, because the statement in the Examiner's Answer includes both phrases. However, Appellants clearly and explicitly state in the Appeal Brief that there are no such appeals or interferences. Reconsideration is respectfully requested.

SUMMARY OF INVENTION

The Examiner's Answer objects to the Summary of the Invention in the Appeal Brief as being deficient. Appellants submit that the summary in the brief and the summary in the Examiner's Answer are sufficient.

ARGUMENT

In response to Appellants' arguments, the Examiner's Answer states:

> Regarding prior art to Noorbakhsh, Appellant argues that Noorbakhsh fails to teach or suggest performing raster operations and writes to video memory on ***a pixel-by-pixel basis***. The examiner agrees and this is why the Examiner added the prior art to Rao.
>
> Regarding prior art to Rao, Appellant argues that Rao also fails to make up for the deficiencies of Noorbakhsh. The examiner disagrees. Rao clearly stated "typical bit block transfer techniques read data from the source block of memory locations ***a word or byte at a time*** (It is noted that a pixel can be any number of bits based on the resolution, such as, a pixel can be 8-bits, 16-bits, 24-bits) and then write that data into the destination block of memory ***a word or byte at a time***" (col. 1, lines 46-50). It is noted that even though Rao did not mention performing "raster operations". Performing raster operations are one of the inherent steps performing during bit block transfer operation (see Noorbakhsh). Therefore, Rao clearly

teaches or make up for the deficiencies of Noorbakhsh.

Examiner's Answer, dated March 8, 2004. Appellants respectfully disagree. The cited portion of *Rao* states:

> In essence, typical bit block transfer techniques read data from the source block of memory locations a word or byte at a time and then write that data into the destination block of memory a word or byte at a time.

Rao, col. 1, lines 46-50. However, *Rao* also states:

> Bit block transfer (BitBLT) is an important performance enhancement technique used in digital data processing, graphics and video applications, and in particular in "windowing" applications. In general, in a bit block transfer ("block move"), an entire block of data (also known as bitmaps) is transferred from a first (source) block of storage locations in display memory to a second (destination) block of storage locations in display memory. In graphics systems BitBLTs can improve operational speed since the data transfers typically remain local to graphics controller thereby reducing the tasks required to be performed by the CPU. Similarly, entire blocks of data may be copied from a set of source locations in memory to a set of destination locations in memory by a block copy.

Rao, col. 1, lines 12-25. Therefore, according to *Rao*, a BitBLT is a technique for moving blocks of data. Within a move of a block, data may be moved a word or a byte at a time. However, *Rao* does not teach that there is any association between a word or a byte and a pixel. While each pixel may be one byte or a word or 24 bits, this would have no effect on **moving** a block of data.

To the contrary, *Rao* is merely describing how data is moved and not how raster operations are performed. In fact, BitBLT is used in *Rao* to easily move image data from one portion of display memory to another portion of display memory. See *Rao*, col. 1, line 53, to col. 2, line 7. There is no suggestion in *Rao* to use BitBLT to read a plurality of picture elements from **system** memory and to read a plurality of picture elements from video memory, as recited in claim 1. Furthermore, there is no suggestion in *Rao* to then perform a raster operation to form a processed picture element, write the processed picture element to video memory, and repeat the performing and writing steps for each picture element. In other words, *Rao* teaches using BitBLT to move data from video memory to video memory as a block, even though the block may be transferred a byte or word at a time. *Rao* does not teach reading a whole block of data from system memory and reading a whole block of data from video memory and then performing raster operations and writes to video memory a picture element at a time.

In contradistinction, the present invention avoids performance degradation that may be experienced when data is read from system memory and video memory, a raster operation is performed, and data is then written to video memory. In the prior art, the system would experience a bus turnaround delay twice for every pixel for such an operation. *Noorbakhsh* uses BitBLT to transfer a whole block of data, perform raster operations on the block of data, and write the block of data to a destination. *Rao* merely teaches moving data from a source to a destination, wherein moving a block may include moving data a bye or word at a time. Thus, *Noorbakhsh* and *Rao*, taken individually or in combination, fail to teach or suggest reading a first plurality of picture elements from the system memory and reading a second plurality of picture elements from the video memory, wherein the first plurality of picture elements and the second plurality of picture elements are selected such that changes in a direction of data on the bus are minimized when performing raster operations on the first plurality of picture elements and the second plurality of picture elements. *Noorbakhsh* and *Rao*, taken individually or in combination, also fail to teach or suggest repeating a step of performing a raster operation and a step of writing a processed picture element for each picture element in the first plurality of picture elements and the second plurality of picture elements until all picture elements have been processed, wherein changes in the direction of data on the bus are minimized between the reading and writing of picture elements, as recited in representative claim 1, for example.

Independent claims 12, 19, and 30 recite subject matter addressed above with respect to claim 1 and are allowable for at least the same reasons. Since claims 2-6, 13-18, and 20-24 depend from claims 1, 12, and 19, the same distinctions between *Noorbakhsh* and *Rao* and the invention recited in claims 1, 12, and 19 apply for these claims.

CONCLUSION

In view of the above, Appellants respectfully submit that the rejection of claims 1-6, 12-24, and 30 is overcome. Accordingly, it is respectfully urged that the rejection of claims 1-6, 12-24, and 30 not be sustained.

Stephen R. Tkacs
Reg. No. 46,430
Yee & Associates, P.C.
PO Box 802333
Dallas, TX 75380
(972) 367-2001